DECLARATION

I, the below-named translator, hereby declare:

(1) That my name, mailing address and citizenship are as stated below;

(2) That I am knowledgeable in the English language and in the Korean language in which Korean Patent Application No. 2000-79375 was filed on December 20, 2000; and

(3) That I have translated said Korean Patent Application No. 2000-79375 into English, whose English text is attached hereto, and believe that said translation is a true and complete translation of the aforementioned Korean patent application.

June 19, 2006

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METHOD AND APPARATUS FOR DRIVING LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a liquid crystal display, and more particularly to a method and apparatus for driving a liquid crystal display wherein a picture quality can be clearly kept upon conversion of a resolution mode of the liquid crystal display.

Description of the Related Art

Generally, a liquid crystal display (LCD) of active matrix driving system uses thin film transistors (TFT's) as switching devices to display a natural moving picture. Since such a LCD can be made into a smaller device in size than the existent Brown tube, it has been widely used for a computer monitor well as office automation equipment such as a copy machine, etc. and portable equipment such as a cellular phone and a pager, etc.

Such a LCD trends toward a high resolution and a large-scale screen. Recently, a liquid crystal monitor of a personal computer has supported resolutions required for high-class equipment such as a workstation. Fig. 1 schematically shows such a LCD.

Referring to Fig. 1, the LCD includes a liquid crystal display panel 2 having TFT's and liquid crystal cells provided between gate lines GL1 to GLm and source lines

SL1 to SLn, a source drive integrated circuit (IC) 6 for supplying a data to the source lines SL1 to SLn, a gate drive IC for sequentially applying scanning pulses to the gate lines GL1 to GLm, a timing controller 8 for applying required timing control signals to the source drive IC 6 and the gate drive IC 4, and an interface circuit 12 for supplying a data from a graphic card (not shown) to the timing controller 8.

The source drive IC 6 samples and latches red (R), green (G) and blue (B) data in response to a source shift clock (SSC) from the timing controller to convert a timing system of 'dot at a time scanning' into that of 'line at a time scanning', then supplies them to the source lines SL1 to SLn.

Timing control signals applied from the timing controller 8 to the source drive IC 6 include a source start pulse (SSP) for instructing an initiation of a data sampling or latch in one horizontal synchronization interval, a source output enable signal (SOE) for controlling an output of the source drive IC 6 and a polarity control signal (POL) for inverting the polarity of a data upon inversion driving, besides the SSC.

The gate drive IC 6 includes a shift register. The gate driver IC 6 sequentially applies scanning pulses having a gate high voltage in response to a gate start pulse (GSP) from the timing controller 8, to thereby charge a data in the liquid crystal cells.

Timing control signals applied from the timing controller 8 to the gate drive IC 4 include a gate shift clock GSC

for determining a time when the gate of the TFT is turned on or off and a gate output enable signal (GOE) for controlling an output of the gate drive IC 4, etc. besides the GSP.

The timing controller 8 receives RGB signals inputted via the interface circuit 12 to distribute it into the source drive IC 6 and control the source drive IC 6 and the gate drive IC 4. The timing controller 8 generates the timing control signals required for the source drive IC 6 and the gate drive IC 4 using the SSC applied from a reference clock generator (not shown).

The interface circuit 12 applies RGB data and a dot clock Dclk from the graphic card (not shown) to the timing controller 8.

The timing controller 8 and the interface circuit 12 may include a LVDS circuit so that they can reduce the number of data supply lines and an electro-magnetic interference.

The VESA (Video Electronics Standard Association) has defined the number of dot clocks Dclk having a frequency of 65Mhz at a blanking interval (or a low logic interval) of a data enable signal I_DE inputted from the graphic card to the timing controller 8 in resolution modes of UXGA, SXGA, XGA, SVGA and VGA by an even number. However, if the resolution mode is converted from UXGA, SXGA or XGA into SVGA or VGA, the number of dot clocks Dclk is changed into an odd number. When the resolution mode is converted, a horizontal noise emerges on the screen.

As can be seen from Fig. 2, the conventional timing

controller 8 toggles a dot clock Dclk from the interface circuit 12 irrespectively of a resolution conversion of the graphic card to generate the SSC. More specifically, the conventional timing controller 8 operates a reset circuit at a dot clock Dclk generated at the third sequence from a time when the data enable signal I_DE is changed into a high level independently of a resolution to reset a source shift clock SSC. Herein, as shown in Fig. 3, if a resolution mode is UXGA, SXGA or XGA, the number of dot clocks Dclk (65Mhz in the XGA mode) at a blanking interval of the data enable signal I_DE is an even number (n). In this case, the source shift clock SSC has normal waveform and frequency. On the other hand, as shown in Fig. 4, if a resolution mode is SVGA or VGA, the number of dot clocks Dclk at a blanking interval of the data enable signal DE is changed into an odd number. As a result, when the resolution mode is converted from UXGA, SXGA or XGA into SVGA or VGA, the source start pulse SSP and the source shift clock SSC inputted to the source shift clock SSC go beyond a timing specification stipulating a set-up time and a hold time to cause a horizontal noise on the screen, as shown in Fig. 5.

In Fig. 3 to Fig. 5, the data enable signal DE is created by an internal circuit of the timing controller 8 to instruct a sampling initiation time of an odd data and an even data divided from an input data by means of the timing controller 8.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method and apparatus for driving a liquid

crystal display wherein a picture quality can be clearly kept upon conversion of a resolution mode of the liquid crystal display irrespective of the number of a dot clock Dclk.

In order to achieve these and other objects of the invention, a method of driving a liquid crystal display according to one aspect of the present invention includes the steps of inputting a data enable signal for indicating a time interval when a video data exists to a controller; detecting an enable initiation time of the data enable signal; generating a reset signal at said enable initiation time of the data enable signal; and resetting a source shift clock by the reset signal.

A driving apparatus for a liquid crystal display according to another aspect of the present invention includes detecting means for detecting an enable initiation time of a data enable signal for indicating a time interval when a vide data exists; and reset means for resetting a source shift clock at said enable initiation time of the data enable signal.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

Fig. 1 is a schematic block diagram showing a configuration of a driving apparatus for a conventional liquid crystal display;

Fig. 2 is an output waveform diagram of the timing

controller shown in Fig. 1;

Fig. 3 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of UXGA, SXGA and XGA;

Fig. 4 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of VGA and SVGA;

Fig. 5 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of XGA and VGA;

Fig. 6 is a schematic block diagram showing a configuration of a source shift clock generator of a timing controller in a driving apparatus for a liquid crystal display according to an embodiment of the present invention;

Fig. 7 is a detailed circuit diagram of the source shift clock generator shown in Fig. 6;

Fig. 8 is an input/output waveform diagram of the driving apparatus for the liquid crystal display according to the embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 6, there is shown a driving apparatus for a liquid crystal display (LCD) according to an embodiment of the present invention.

The driving apparatus for LCD includes a source shift clock (SSC) reset unit 20 and a reference clock generator 30. The source shift clock (SSC) reset unit 20 receives a dot clock Dclk and a data enable signal I_DE to generate a reset signal (RESET) at a time when a data enable signal I_DE is changed into a high level. The reference clock

generator 30 resets the source shift clock (SSC) at the time when a data enable signal I_DE is changed into a high level. The source shift clock (SSC) reset unit 20 and the reference clock generator 30 can be formed within the timing controller 8, or they can be formed as independent circuits.

The SSC reset unit 20 detects a time when a data enable signal (I_DE) is changed into a high level irrespectively of the number of dot clocks (Dclk) upon conversion of a resolution mode to generate a reset signal (RESERT). As shown in Fig. 7, the SSC reset unit 20 includes a D flip-flop 21 receiving the data enable signal I_DE and the dot clock (Dclk) from the interface circuit 12, an inverter 23 connected to an output terminal of the D flip-flop 21, a buffer 22 receiving a data enable signal (I_DE) via an I_DE input line 26, an AND gate commonly connected to output terminals of the buffer 22 and the inverter 23, and a reset part 25 connected between a Dclk input line 27 and the output terminal of the AND gate 24. The D flip-flop 21 outputs a data enable signal (I_DE) inputted into the timing controller 8 whenever the dot clock (Dclk) is inputted. The buffer 22 applies a data enable signal I_DE inputted via the I_DE input line 26 to a first input terminal of the AND gate 24 by buffering. The inverter 23 logically inverts a square wave inputted from the D flip-flop 21 and applies it to a second input terminal of the AND gate 24. The AND gate 24 makes a logical product operation of the data enable signal (I_DE) from the buffer 22 and the inverted data enable signal (I_DE) from the inverter 23 to generate a signal indicating a time when the data enable signal (I_DE) is changed from a low logic into a high logic. The reset part 25 generates a reset

signal to reset a source shift clock (SSC) in response to the high logic signal inputted from the AND gate 24. The reference clock generator 30 generates a source shift clock (SSC) and resets the source shift clock (SSC) at the time when the data enable signal (I_DE) is changed from a low logic into a high logic in response to the reset signal supplied from the reset part 25.

The operation of the source shift clock (SSC) reset unit 20 will be explained in connection with Fig. 8.

Referring to Fig. 8, the dot clock Dclk of 65Mhz is commonly inputted to the D flip-flop 21 and the reset part 25 to synchronize a signal outputted from the AND gate 24 with a signal outputted from the reset part 25. If the data enable signal (I_DE) is at a blanking interval that is, has a low logic, then an output signal of the AND gate 24 remains at a low logic because an output signal of the buffer 22 maintains a low logic. Since output signals of the buffer 22 and the inverter 23 have a high logic simultaneously at a time when the data enable signal (I_DE) is changed from a low logic into a high logic, the AND gate 24 generates a pulse signal having high logic. In other words, the AND gate 24 detects a time when a logic value of the data enable signal (I_DE) is changed from a low logic into a high logic irrespectively of a change in the number of dot clocks upon conversion of a resolution mode, for example, upon conversion from UXGA, SXGA or XGA into SVGA or VGA. The pulse signal generated from the AND gate 24 in this manner is applied to the reset part 25 to reset a source shift clock (SSC) of 32.5Mhz outputted from the reference clock generator 30. Accordingly, the source shift clock (SSC) inputted to the source drive IC 66

always has a normal pulse width and frequency in an enable interval of the data enable signal (I_DE) regardless of a conversion of a resolution mode. The source start pulse (SSP) is generated at twice pulse width of the source shift clock (SSC) between the odd and even data and the reset signal by means of the timing controller 8.

As described above, according to the present invention, an initiation time of an enabling interval of the data enable signal I_DE inputted to the timing controller is detected irrespectively of an odd/even change of the dot clock Dclk caused by a resolution conversion to reset the source shift clock (SSC). As a result, the source shift clock (SSC) and the source start pulse (SSP) inputted to the source drive IC meets a timing specification in the VESA standard independently of an odd/even change of the dot clock (Dclk) upon conversion of a resolution mode, for example, upon conversion from UXGA, SXGA or XGA mode into SVGA or VGA mode, so that it becomes possible to prevent a generation of horizontal noise upon conversion of a resolution mode. Furthermore, according to the present invention, timing margins of the source shift clock (SSC) and the source start pulse (SSP) inputted to the source drive IC are assured, so that it becomes possible to keep a clear picture under a low temperature or high temperature environment.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the

invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A method of driving a liquid crystal display having a controller for generating a source shift clock and a source start pulse to control a source drive circuit, comprising the steps of:

inputting a data enable signal for indicating a time interval when a video data exists to the controller;

detecting an enable initiation time of the data enable signal;

generating a reset signal at said enable initiation time of the data enable signal; and

resetting the source shift clock for sampling the video data by the reset signal.

2. A driving apparatus for a liquid crystal display having a controller for generating a source shift clock and a source start pulse to control a source drive circuit, comprising:

detecting means for detecting an enable initiation time of a data enable signal for indicating a time interval when a vide data exists; and

reset means for resetting a source shift clock at said enable initiation time of the data enable signal.

3. The driving apparatus according to claim 2, further comprising:

a D flip-flop for receiving the data enable signal and outputting the data enable signal in response to a dot clock; and

an inverter for logically inverting the data enable signal;

an AND gate for making a logical product operation of

the inverted enable signal and the data enable signal to generate a reset signal for indicating an enable initiation time of the data enable signal.

Abstract

A method and apparatus for driving a liquid crystal display wherein a picture quality can be clearly kept upon conversion of a resolution mode of the liquid crystal display when a picture quality mode is converted. The present invention detects an enable initiation time of the data enable signal and generates a reset signal at said enable initiation time of the data enable signal, then resets the source shift clock by the reset signal.

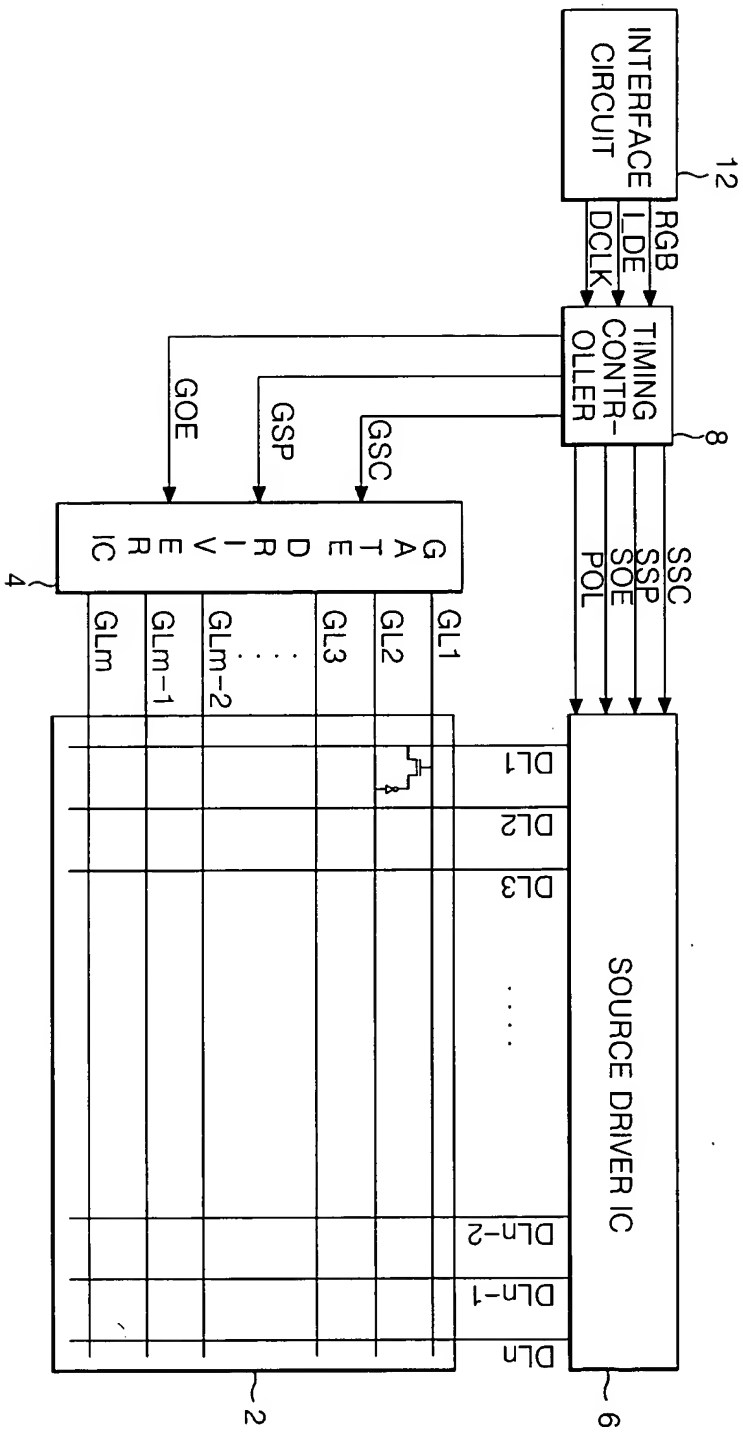

FIG. 1
RELATED ART

FIG.2
RELATED ART

Video Mode	N	PinName
	1	Dclx [XGA: 65MHz] (Falling Egde 에서 Latch)
	2	Video Data
	3	Data Lactch
	4	Toggle at Dclk Rising
	5	Odd Data La1ch
	6	FOUR TIMES Toggle SIGNAL INVERSION
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS EVEN NUMBER(n)	7	Even Data Latch
	8	FOUR TIMES Toggle SIGNAL INVERSION
	9	Even Data Latch
	10	FOUR TIMES Toggle SIGNAL INVERSION
	11	Even Data {D-IC INPUT Video Signal}
	12	Odd Data {D-IC INPUT Video Signal}
	13	Odd Enable
	14	SSC
	15	FOUR TIMES Toggle SIGNAL INVERSION
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS ODD NUMBER(n+1)	16	Even Data {D-IC INPUT Video Signal}
	17	Odd Data {D-IC INPUT Video Signal}
	18	Data Enable
	19	SSP

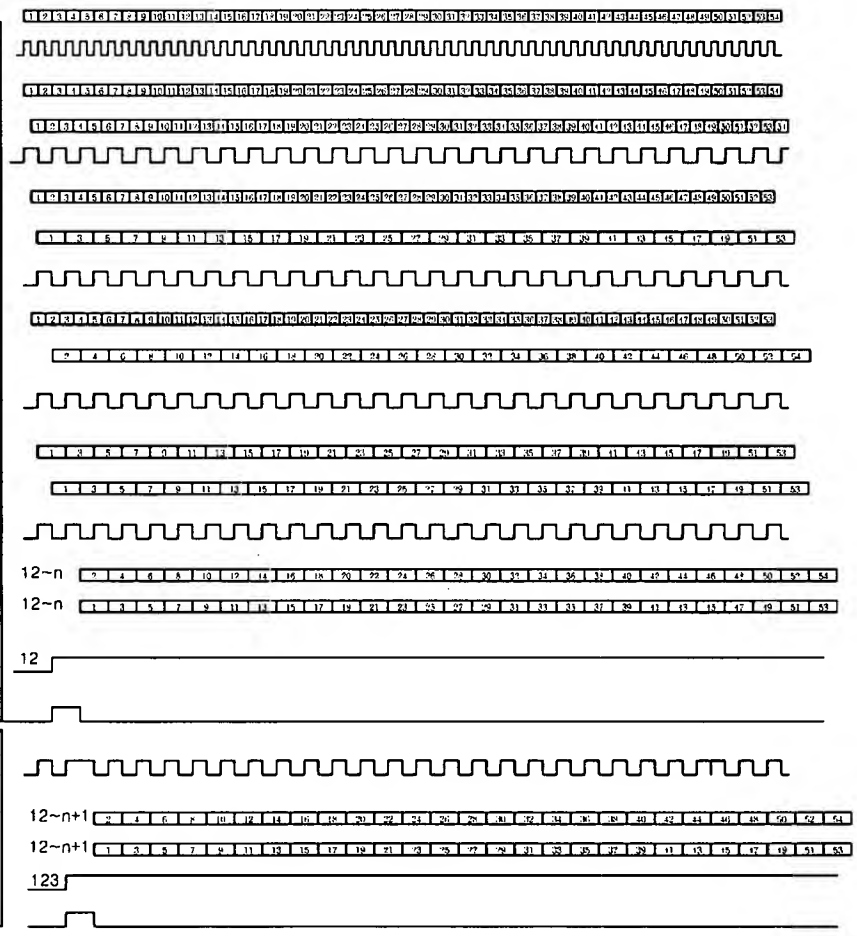

FIG.3
RELATED ART

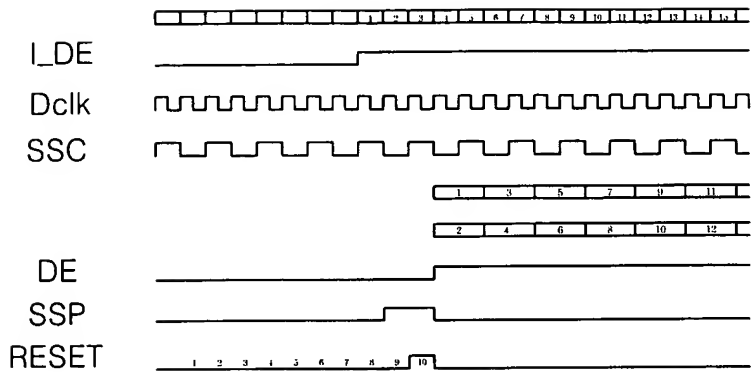

FIG.4
RELATED ART

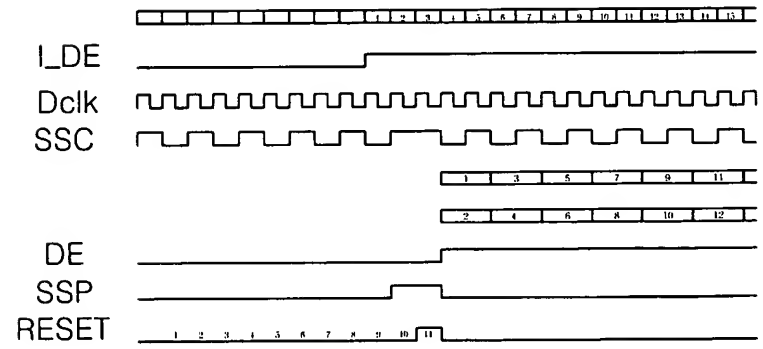

FIG.5

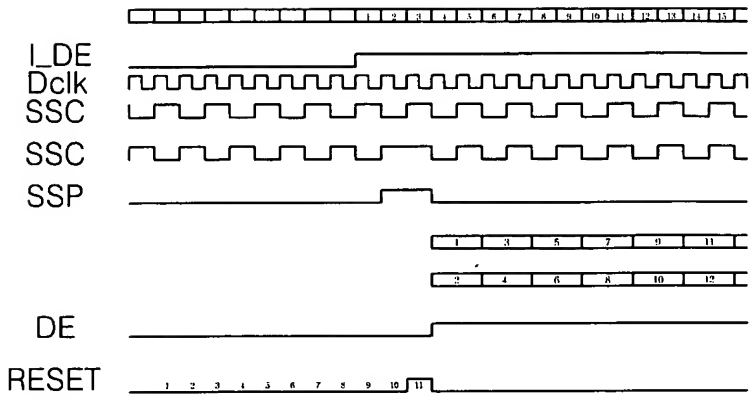

FIG.6

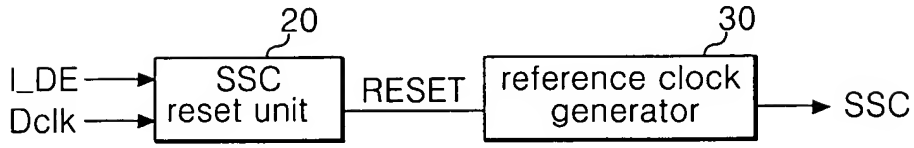

FIG. 7

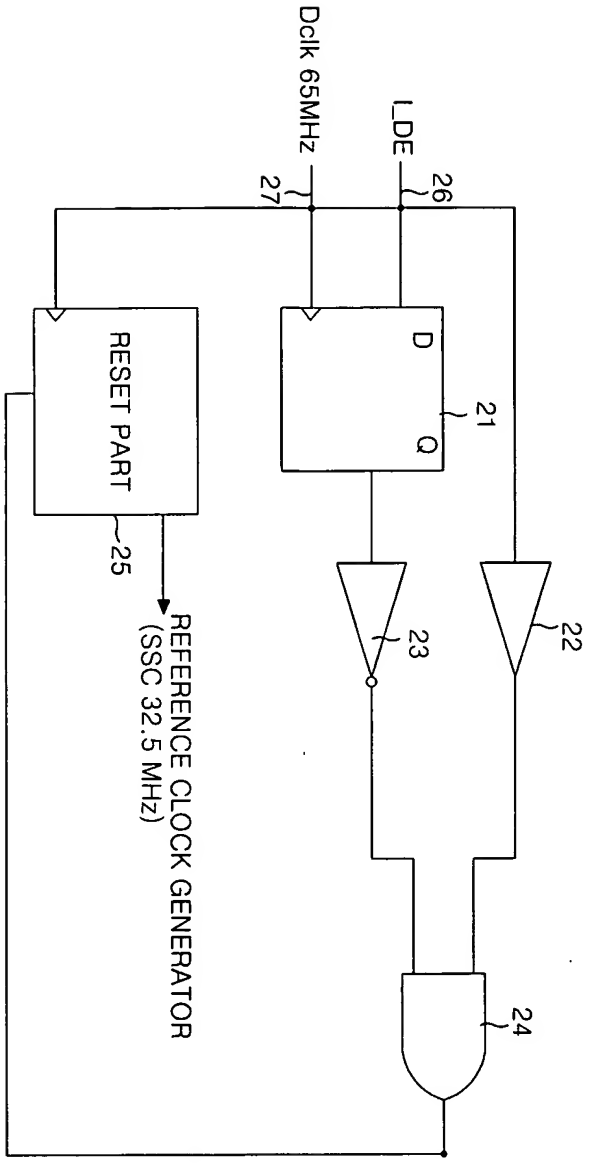
Dclk 65MHz
27
I_DE
26
D
Q
21
RESET PART
25
22
23
24
REFERENCE CLOCK GENERATOR
(SSC 32.5 MHz)

FIG.8